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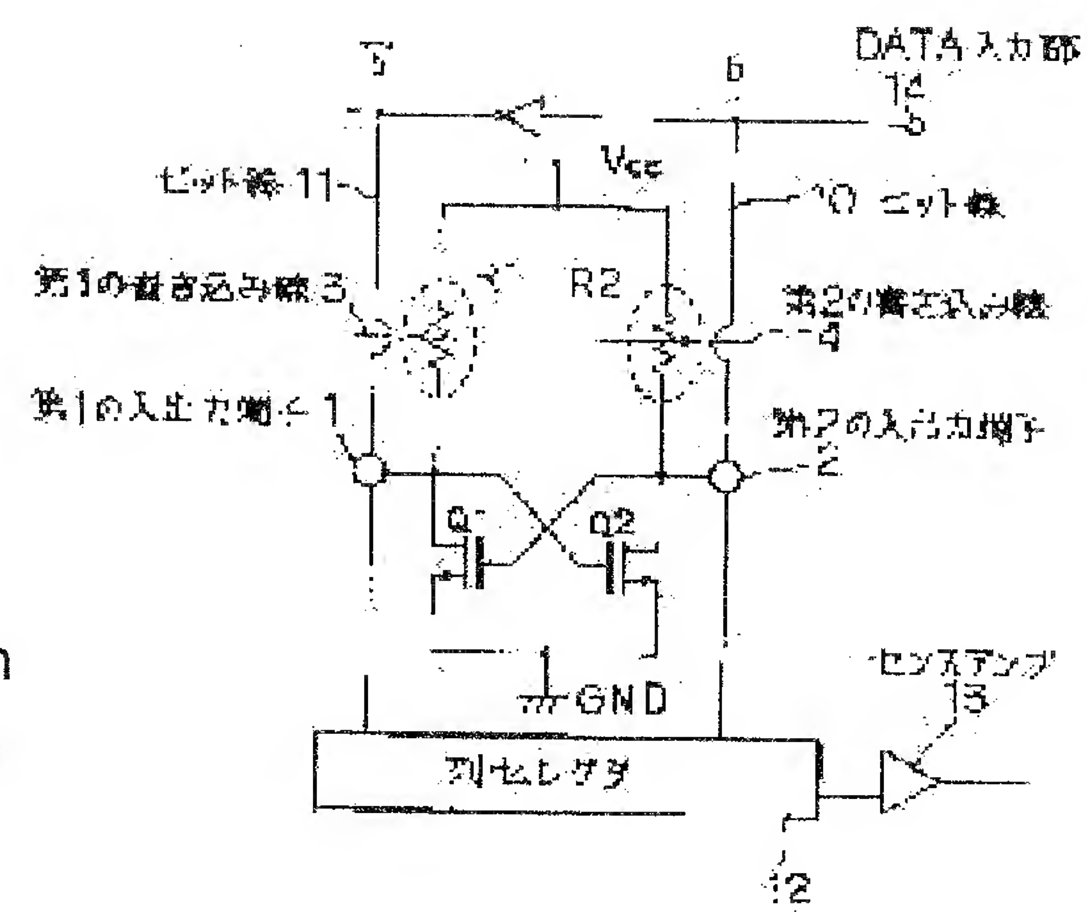
(54) SEMICONDUCTOR MEMORY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor memory device consisting of nonvolatile memory cells equipped with magneto-resistance elements such as a GMR element and a TMR element in which the number of times of repeat writing is reduced and the service life of the device is improved.



SOLUTION: The memory cell is provided with a first MOS transistor and a second MOS transistor in which a sauce is grounded and a gate is connected to each other's drain, a first magneto resistance element inserted between the drain of the first MOS transistor and a power source line, and a second magneto resistance element inserted between the drain of the second MOS transistor and the power source line. The memory cell has further a first write means which applies a specified voltage to the gate of the first MOS transistor and the gate of the second MOS transistor according to write information, respectively, and a read means which detects the electrical potential of the drain of the first MOS transistor and the drain of the second MOS transistor to read information.

CLAIMS

[Claim(s)]
[Claim 1]A semiconductor memory device comprising provided with two or more memory cells:
The 1st and 2nd MOS transistors by which sauce was grounded by said memory cell and a gate was connected to a drain of another side at it, respectively.
A drain of said 1st MOS transistor, and the 1st magnetic resistance element inserted between power source wires.
A drain of said 2nd MOS transistor, and the 2nd magnetic resistance element inserted between said power source wires.
The 1st writing means that impresses voltage more than threshold voltage of a MOS transistor to either of the gates of said 1st or 2nd MOS transistor according to information written in to a preparation and said memory cell, A reading means which reads information written in said memory cell by detecting drain potential of said 1st and 2nd MOS transistors, respectively.

[Claim 2]The semiconductor memory device according to claim 1 which is an element from which said 1st magnetic resistance element and the 2nd magnetic resistance element have two magnetic layers which differ in holding power, and the non-magnetic layer pinched between said magnetic layers, and resistance differs by a relative magnetizing direction of said two magnetic layers.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the semiconductor memory device provided with the nonvolatile memory cell containing magnetic resistance elements, such as a GMR (Giant Magneto-Resistance) element and a TMR (spin TunnelingMagneto-Resistance) element.
[0002]
[Description of the Prior Art]Conventionally, SRAM (Static Random Access Memory) is well known as a semiconductor memory device in which read-out/writing of information are possible at high speed. Hereafter, it explains, using drawing 9 about the memory cell of SRAM as the 1st conventional example of a semiconductor memory device.

TECHNICAL FIELD

[Field of the Invention]This invention relates to the semiconductor memory device provided with the nonvolatile memory cell containing magnetic resistance elements, such as a GMR (Giant Magneto-Resistance) element and a TMR (spin TunnelingMagneto-Resistance) element.

[Translation done.]

PRIOR ART

[Description of the Prior Art]Conventionally, SRAM (Static Random Access Memory) is well known as a semiconductor memory device in which read-out/writing of information are possible at high speed. Hereafter, it explains, using drawing 9 about the memory cell of SRAM as the 1st conventional example of a semiconductor memory device.
[0003]Drawing 9 is a circuit diagram showing the composition of the memory cell of SRAM which is a semiconductor memory device of the 1st conventional example.
[0004]As shown in drawing 9, the memory cell of SRAM, The 1st MOS transistor Q11 and 2nd MOS transistor Q12 by which sauce was grounded and the gate was connected to the drain of another side, respectively, It is the composition of having a drain of 1st MOS transistor Q11, 1st load R_{L1} inserted between power source wires, and the drain of 2nd MOS transistor Q12 and 2nd load R_{L2} inserted between power source wires.
[0005]The 1st input/output terminal 11 is connected to the drain of 1st MOS transistor Q11, and the 2nd input/output terminal 12 is connected to the drain of 2nd MOS transistor Q12.
[0006]In such composition, when writing information in the memory cell shown in drawing 9, the voltage which changes in the 1st input/output terminal 11 and 2nd input/output terminal 12 with unillustrated writing means, respectively is impressed. The impressed electromotive force to the 1st input/output terminal 11 is more than the threshold voltage of a MOS transistor here, When the impressed electromotive force to the 2nd input/output terminal 12 is lower than the threshold voltage of a MOS transistor, 2nd MOS transistor Q12 turns on, the potential of the 2nd input/output terminal 12 is fixed to earth-potentials GND, 1st MOS transistor Q11 turns off and the potential of the 1st input/output terminal 11 is fixed to the power supply potential Vcc.
[0007]On the contrary, the impressed electromotive force to the 1st input/output terminal 11 is lower than the threshold voltage of a MOS transistor, When the impressed electromotive force to the 2nd input/output terminal 12 is more than the threshold voltage of a MOS transistor, 2nd MOS transistor Q12 turns off, the potential of the 2nd input/output terminal 12 is fixed to the power supply potential Vcc, 1st MOS transistor Q11 turns on and the

potential of the 1st input/output terminal 11 is fixed to earth-potentials GND.

[0008]Therefore, information is recordable as binary data by which potential of the 1st input/output terminal 11 or the 2nd input/output terminal 12 is high. Such a state is held as long as the power supply is supplied, if new information is not written in. The output potential of the 1st input/output terminal 11 and the 2nd input/output terminal 12, Since it is amplified by the MOS transistor and fixed to the power supply potential Vcc or earth-potentials GND, It is possible to fully secure potential difference required for detection of information, and read operation of the information by an unillustrated reading means is made easy, and high-speed read-out/writing operation become possible.

[0009]Next, the memory cell provided with magnetic resistance elements, such as a GMR element or a TMR element, as the 2nd conventional example of a semiconductor memory device is explained using drawing 10.

[0010]Drawing 10 is a circuit diagram showing the composition of the memory cell provided with the magnetic resistance element which is a semiconductor memory device of the 2nd conventional example.

[0011]As shown in drawing 10, the memory cell of the 2nd conventional example, The 1st magnetic resistance element R21 and 2nd magnetic resistance element R22 by which one terminal was grounded, respectively, It is the composition of having a terminal of another side of the 1st magnetic resistance element R21, 1st MOS transistor Q21 inserted between current supply source lines, and the terminal of another side of the 2nd magnetic resistance element R22 and 2nd MOS transistor Q22 inserted between current supply source lines.

[0012]The drain of 1st MOS transistor Q21 and 2nd MOS transistor Q22 is connected with a current supply source line, respectively, The sauce of 1st MOS transistor Q21 is connected with the terminal of another side of the 1st magnetic resistance element R21, and the sauce of 2nd MOS transistor Q22 is connected with the terminal of another side of the 2nd magnetic resistance element R22. The gate of 1st MOS transistor Q21 and 2nd MOS transistor Q22 is connected to the control terminal 21 in common, respectively.

[0013]The 1st magnetic resistance element R21 and 2nd magnetic resistance element R22 are the composition of having two magnetic layers which consist of a GMR element or a TMR element, and differ in coercive force, respectively, and the non-magnetic layer pinched among them. The 1st magnetic resistance element R21 and 2nd magnetic resistance element R22 are an element which shows resistance which is different by whether the magnetizing direction of these two magnetic layers is a uniform direction, or it is an opposite direction.

[0014]The 1st write-in line 22 for controlling the magnetizing direction of the magnetic layer of the 1st magnetic resistance element R21 in the 1st magnetic resistance element R21 and the approaching position is formed, The 2nd write-in line 23 for controlling the magnetizing direction of the magnetic layer of the 2nd magnetic resistance element R22 is formed in the 2nd magnetic resistance element R22 and the approaching position.

[0015]When writing information in the memory cell shown in drawing 10 in such

composition, Write current is sent in the direction opposite to the 1st write-in line 22 and the 2nd write-in line 23 by an unillustrated writing means, and a magnetic layer is made to magnetize by the magnetic field generated to the circumference of a write-in line so that the resistance of the 1st magnetic resistance element R21 and the 2nd magnetic resistance element R22 may differ.

[0016]Information is recordable as binary data by which resistance of this 1st magnetic resistance element R21 or the 2nd magnetic resistance element R22 is large. Since it does not change even if it turns off a power supply, if the resistance of the 1st magnetic resistance element R21 and the 2nd magnetic resistance element R22 does not write in new information, respectively, the memory cell shown in drawing 10 functions as a nonvolatile memory cell.

[0017]On the other hand, when reading information from the memory cell shown in drawing 10, By an unillustrated reading means, predetermined voltage is impressed to the control terminal 21, the 1st MOS transistor Q21 and 2nd MOS transistor Q22 are made to turn on, and the respectively same voltage is impressed to the 1st magnetic resistance element R21 and 2nd magnetic resistance element R22. The current according to each resistance flows into the 1st magnetic resistance element R21 and 2nd magnetic resistance element R22 at this time, Since current difference arises in current I_{21} which flows into the 1st magnetic resistance element R21, and current I_{22} which flows into the 2nd magnetic resistance element, the information written in by detecting this current difference by a reading means can be read.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention]Since this invention is constituted as explained above, the effect indicated below is done so.
[0072]The 1st and 2nd MOS transistors by which sauce was grounded by the memory cell and the gate was connected to the drain of another side at it, respectively, By having a drain of the 1st MOS transistor, the 1st magnetic resistance element inserted between power source wires, and the drain of the 2nd MOS transistor and the 2nd magnetic resistance element inserted between power source wires. Like the memory cell of SRAM, the read operation of information is easy and high-speed read-out/writing operation become possible.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, among the conventional semiconductor memory devices which were described above, since the memory cell of SRAM of the 1st conventional example is a volatile memory cell, the information currently written in while the power supply was disconnected will be lost. On the other hand, in the memory cell provided with the magnetic resistance element of the 2nd conventional example, since information is rewritten by changing the magnetizing direction of a magnetic layer, we are anxious about disappearance of the information by creep by change of a frequent magnetizing direction. Creep is a phenomenon which a magnetizing direction comes to reverse automatically, when the magnetizing direction of the magnetic layer of a GMR element or a TMR element is changed exceeding predetermined repetition writing frequencies (the maximum repetition writing frequencies).
[0019]This invention is made in order to solve the problem which a Prior art which was described above has, and it is a thing.
It is providing the semiconductor memory device which consists of a nonvolatile memory cell provided with magnetic resistance elements which reduced the purpose and raised the device life, such as a GMR element and a TMR element.

[Translation done.]

MEANS

[Means for Solving the Problem]In order to attain the above-mentioned purpose a semiconductor memory device of this invention, The 1st and 2nd MOS transistors by which were been the semiconductor memory device provided with two or more memory cells, and sauce was grounded by said memory cell and a gate was connected to a drain of another side at it, respectively, A drain of said 1st MOS transistor, and the 1st magnetic resistance element inserted between power source wires, A drain of said 2nd MOS transistor, and the 2nd magnetic resistance element inserted between said power source wires, The 1st writing means that impresses voltage more than threshold voltage of a MOS transistor to either of the gates of said 1st or 2nd MOS transistor according to information written in to a preparation and said memory cell, A reading means which reads information written in said memory cell by detecting drain potential of said 1st and 2nd MOS transistors, respectively, It is the composition of ****(ing) and said 1st magnetic resistance element and the 2nd magnetic resistance element are elements which have two magnetic layers which differ in holding power, and the non-magnetic layer pinched between said magnetic layers and from which resistance differs by a relative magnetizing direction of said two magnetic layers.
[0021]The 1st write-in line that makes a determined direction magnetize at least one magnetic layer of said 1st magnetic resistance element by a magnetic field generated here because current flows, The 2nd write-in line that makes a determined direction magnetize at least one magnetic layer of said 2nd magnetic resistance element by a magnetic field generated because current flows, A potential detection means to detect potential of a drain of said 1st and 2nd MOS transistors before cutting of power supply voltage to said power source wire, respectively, The 2nd writing means that sends predetermined current through said 1st write-in line and/or said 2nd write-in line according to potential relation of a drain of said 1st and 2nd MOS transistors detected by said potential detection means, respectively, An information reproduction means which impresses predetermined voltage to a gate of said 1st and 2nd MOS transistors after current supply to said power source wire according to resistance of said 1st and 2nd magnetic resistance elements, respectively, Composition which **** is preferred, and since that it is a TMR element has the large rate of a

magnetoresistance change, said 1st magnetic resistance element and the 2nd magnetic resistance element have it. [preferred]
[0022]Since it can miniaturize a memory cell that it is the composition that a magnetic layer is magnetized by film surface perpendicular direction, said 1st magnetic resistance element and the 2nd magnetic resistance element have it. [preferred]
[0023]Since it can miniaturize a semiconductor memory device that it is the composition that said 1st write-in line and the 2nd write-in line which are arranged corresponding to a memory cell of a column direction among said two or more memory cells arranged in the shape of a lattice were communalized, it is preferred.
[0024]A semiconductor memory device of this invention is a semiconductor memory device provided with two or more memory cells, . One input and an output of another side were connected to said memory cell, respectively, and a flip-flop was constituted. It has a power source wire, a MOS transistor, and the 1st and 2nd inverters that consist of variable resisters, The 1st writing means that impresses voltage more than threshold voltage of this MOS transistor to either of the gates of said MOS transistor according to information written in to said memory cell, It is the composition of having the 2nd writing means that records information by changing a resistor of said variable resister.
[0025]Here, since read-out/writing of as opposed to a memory cell in it being a magnetic resistance element of information become high-speed and can constitute a nonvolatile memory cell, said variable resister is preferred.
[0026]
[Embodiment of the Invention]Next, this invention is explained with reference to drawings.
[0027]Drawing 1 is a circuit diagram showing the example of 1 composition of the memory cell which the semiconductor memory device of this invention has.
[0028]As shown in drawing 1, the memory cell with which the semiconductor memory device of this invention is provided, The 1st MOS transistor Q1 and 2nd MOS transistor Q2 by which sauce was grounded and the gate was connected to the drain of another side, respectively, It is the composition of having a drain of 1st MOS transistor Q1, the 1st magnetic resistance element R1 inserted between power source wires, and the drain of 2nd MOS transistor Q2 and the 2nd magnetic resistance element R2 inserted between power source wires.
[0029]The 1st inverter is formed with the power source wire connected to the 1st MOS transistor Q1, 1st magnetic resistance element R1, and power supply, The 2nd inverter is formed, the input of one inverter and the output of the inverter of another side are connected by the power source wire connected to 2nd MOS transistor Q2, the 2nd magnetic resistance element R2, and a power supply, respectively, and the flip-flop (connected annularly) is constituted with it. While the power supply is supplied, information is held by this flip-flop composition.

EXAMPLE

(The 1st example) Drawing 5 is a top view showing the composition of the 1st example of the semiconductor memory device provided with the memory cell shown in drawing 1. Drawing 5 shows signs that the control line connected with a MOS transistor, the 2nd MOS transistor, and the 1st input/output terminal and 2nd input terminal was omitted, respectively. [1st]
[0056]As shown in drawing 5, the semiconductor memory device of this example is the composition that two or more memory cells shown in drawing 1 have been arranged in the shape of a lattice. The 1st write-in line 3 is arranged at the position which approaches the column direction of each memory cell arranged in the shape of a lattice with the 1st magnetic resistance element R1, and the 2nd write-in line 4 is arranged at the 2nd magnetic resistance element R2 and the approaching position. The 3rd write-in line 5 is arranged at the position which approaches the 1st magnetic resistance element R1 and 2nd magnetic resistance element R2 at the line writing direction of each memory cell 10 arranged in the shape of a lattice, respectively.
[0057]In such composition, when writing in information, A power supply is supplied from the power supply circuit 7 so that a magnetic field may be impressed in the direction opposite to the 1st magnetic resistance element R1 and 2nd magnetic resistance element R2 corresponding to the selected memory cell, Write current I_1 and I_2 flow into the 1st write-in line 3 and the 2nd write-in line 4, respectively. A power supply is simultaneously supplied also to the 3rd write-in line 5 corresponding to the selected memory cell from the power supply circuit 8, and write current I_3 flows. In order that the 3rd write-in line 5 may just act as a writing means for impressing an auxiliary magnetic field to the selected memory cell, the current of only one way should just flow.
[0058]The magnetizing direction of the 1st magnetic layer of each magnetic resistance element, It is set up in the controllable direction by the synthetic magnetic field of the magnetic field generated in current I_1 which flows into the 1st write-in line 3 of a column

direction, and the 2nd write-in line 4, and I_2, and the magnetic field generated in current I_3 which flows into the 3rd write-in line 5 of a line writing direction.

[0059]Other composition of the semiconductor memory device of this example is shown in drawing 6.

[0060]Drawing 6 is a top view showing other composition of the 1st example of the semiconductor memory device provided with the memory cell shown in drawing 1.

[0061]It is the composition that the 1st write-in line 3 and the 2nd write-in line 4 were connected at each end, and write-in wiring was turned up in the semiconductor memory device shown in drawing 6. In this case, since the current for reverse flows into the 1st write-in line 3 and the 2nd write-in line 4 mutually, two magnetic resistance elements in each memory cell can be set as a different magnetized state.

[0062]Therefore, according to the semiconductor memory device of this example, read-out/writing of information can be performed to the memory cell of the request of two or more memory cells arranged in the shape of a lattice.

[0063]Where a power supply is disconnected in the conventional SRAM, maintenance of information was not completed, but since information is held by a magnetic resistance element, it can become possible to hold information at the time of powering off, and it can be made to function as an unvolatilized memory cell in the semiconductor memory device of this example. In the semiconductor memory device of this example, since the creep about which we are anxious by changing the magnetizing direction of a magnetic resistance element frequently can also reduce the number of times of flux reversal substantially, it can raise the endurance (device life) as a semiconductor memory device.

[0064]In the usual SRAM, since the MOS transistor of the inverter which is always one side is an ON state, there is a fault which a direct current flows regularly and consumes current. In the semiconductor memory device of this example, such a problem is solvable by changing maintenance of information from the flip flop operation by an inverter to a magnetic resistance element. For example, when rewriting of the information on a certain fixed time memory cell is not performed, power consumption can be reduced by forming the means for changing to the information maintenance by a magnetic resistance element in the control circuit 9 shown in drawing 5.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a circuit diagram showing the example of 1 composition of the memory cell which the semiconductor memory device of this invention has.
[Drawing 2]It is a figure showing the structure of the magnetic resistance element which consists of GMR elements, and the sectional view in which a magnetizing direction shows a horizontal example to a magnetic layer side, and the figure (b) of the figure (a) are sectional views in which a magnetizing direction shows a vertical example to a magnetic layer side.
[Drawing 3]It is a figure showing the structure of the magnetic resistance element which consists of TMR elements, and the sectional view in which a magnetizing direction shows a horizontal example to a magnetic layer side, and the figure (b) of the figure (a) are sectional views in which a magnetizing direction shows a vertical example to a magnetic layer side.
[Drawing 4]It is a figure showing how for the magnetic resistance element shown in drawing 1 to write in information, and is a mimetic diagram in which the mimetic diagram and the Drawing (c) and (d) in which the Drawing (a) and (b) shows a situation when a magnetizing direction is level to a magnetic layer side show a situation when a magnetizing direction is vertical to a magnetic layer side.
[Drawing 5]It is a top view showing the example of 1 composition of the semiconductor memory device provided with the memory cell shown in drawing 1.
[Drawing 6]It is a top view showing other composition of the 1st example of the semiconductor memory device provided with the memory cell shown in drawing 1.
[Drawing 7]It is a top view showing the composition of the 2nd example of the semiconductor memory device provided with the memory cell shown in drawing 1.
[Drawing 8]It is a mimetic diagram showing the section which looked at the memory cell with which the semiconductor memory device shown in drawing 7 is provided from the A-A' line.
[Drawing 9]It is a circuit diagram showing the composition of the memory cell of SRAM which is a semiconductor memory device of the 1st conventional example.
[Drawing 10]It is a circuit diagram showing the composition of the memory cell provided

with the magnetic resistance element which is a semiconductor memory device of the 2nd conventional example.

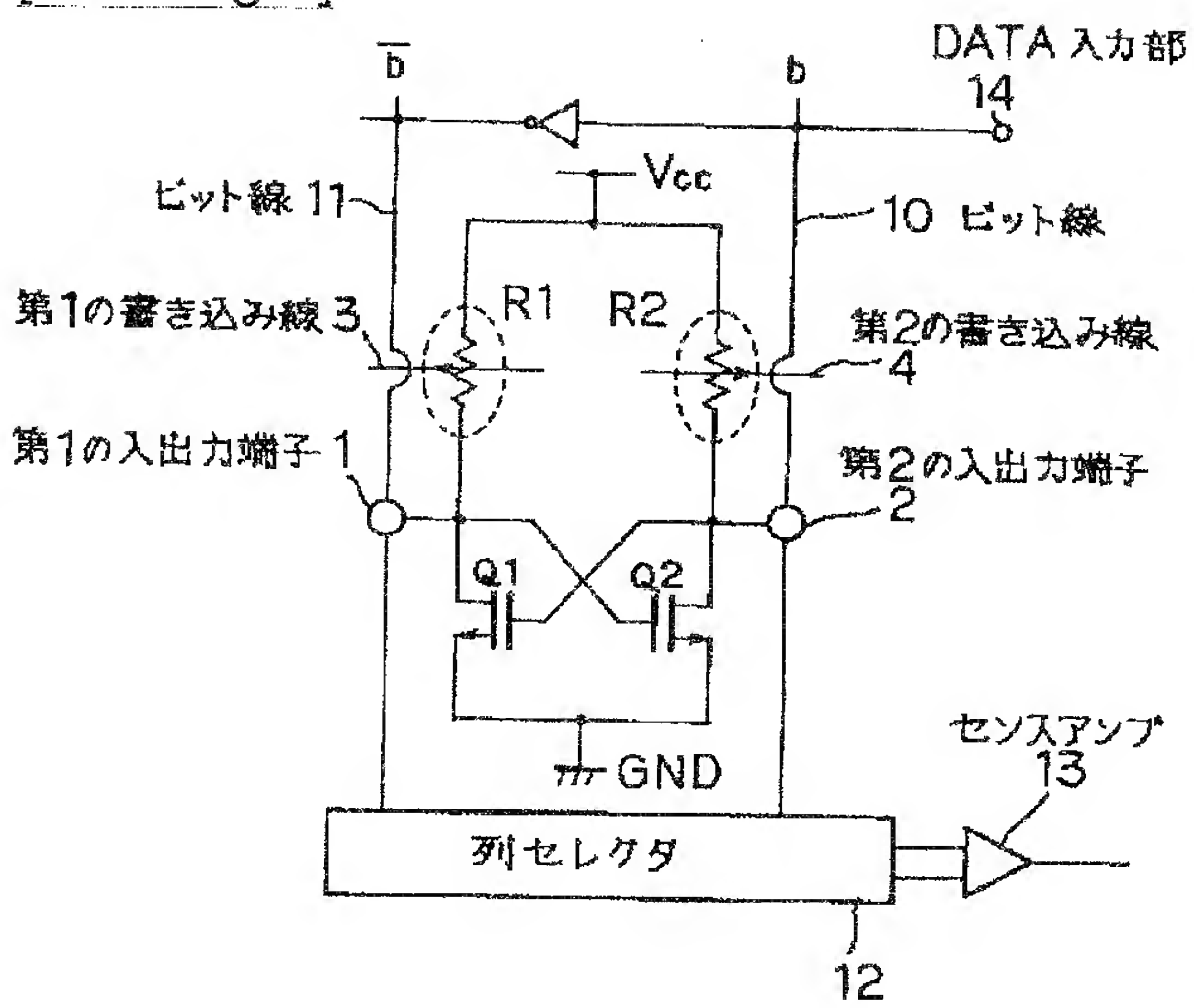
[Description of Notations]

1 The 1st input/output terminal
2 The 2nd input/output terminal
3 The 1st write-in line
4 The 2nd write-in line
5 The 3rd write-in line
7 and 8 Power supply circuit
9 Control circuit
10, 11 bit lines
12 Sequence selector
13 Sense amplifier
14 DATA input part
101 and 111 The 1st magnetic layer
102 and 112 The 2nd magnetic layer
103 and 113 Non-magnetic layer
104 and 114 Electrode
200 A write-in line
Q1 The 1st MOS transistor
Q2 The 2nd MOS transistor
R1 The 1st magnetic resistance element
R2 The 2nd magnetic resistance element

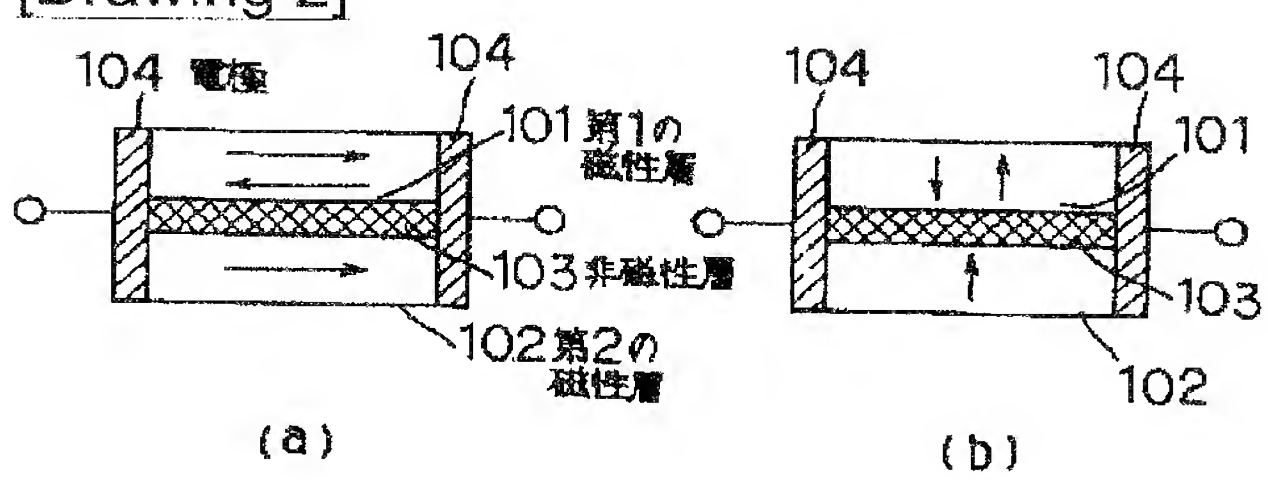
[Translation done.]

DRAWINGS

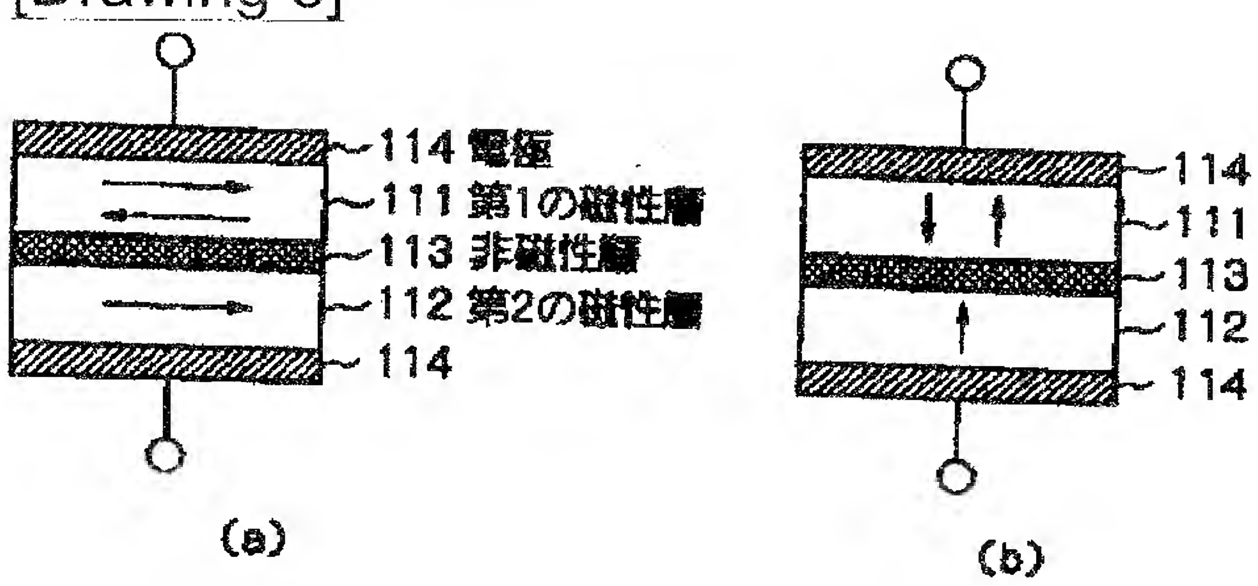
[Drawing 1]



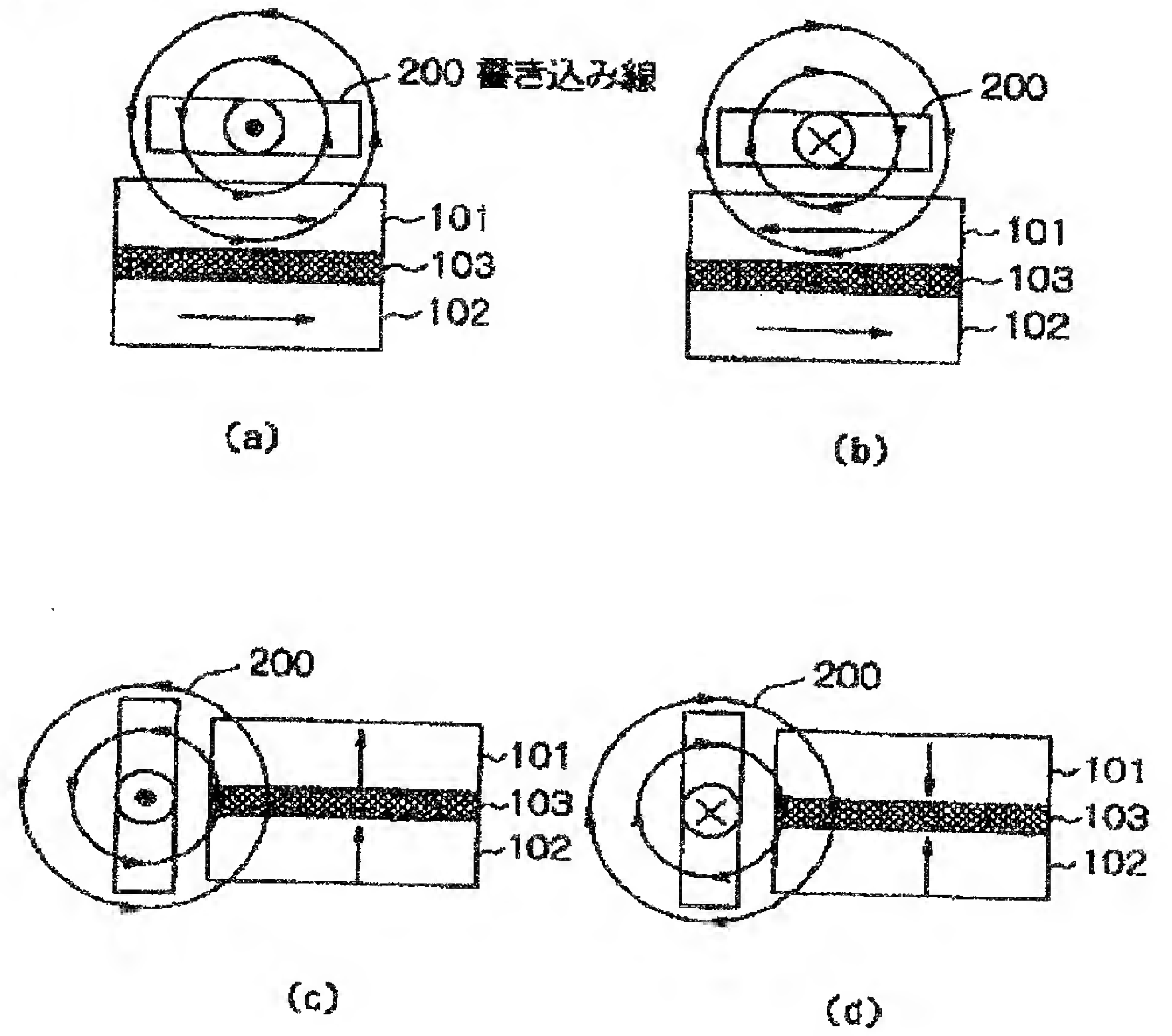
[Drawing 2]



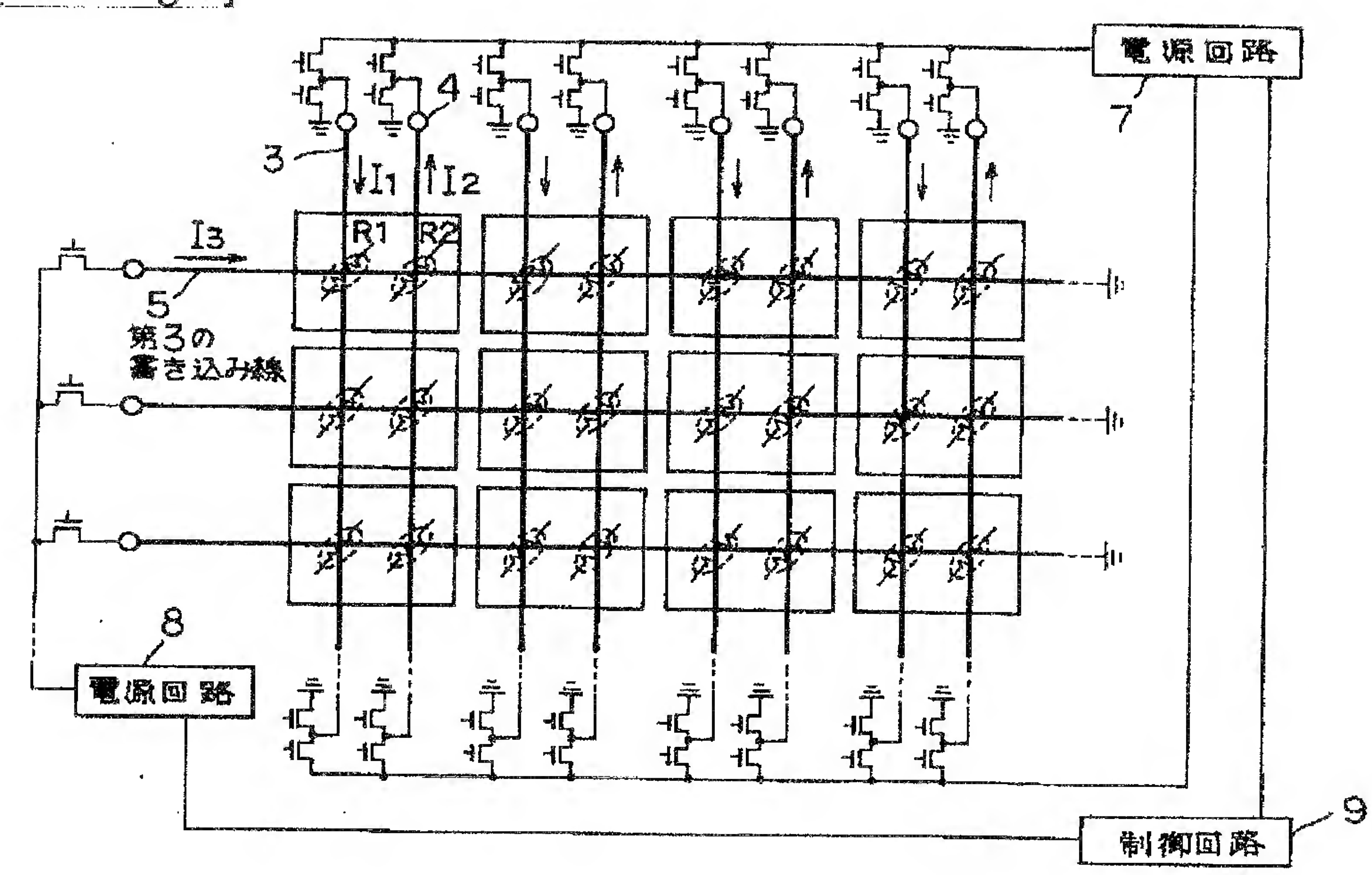
[Drawing 3]



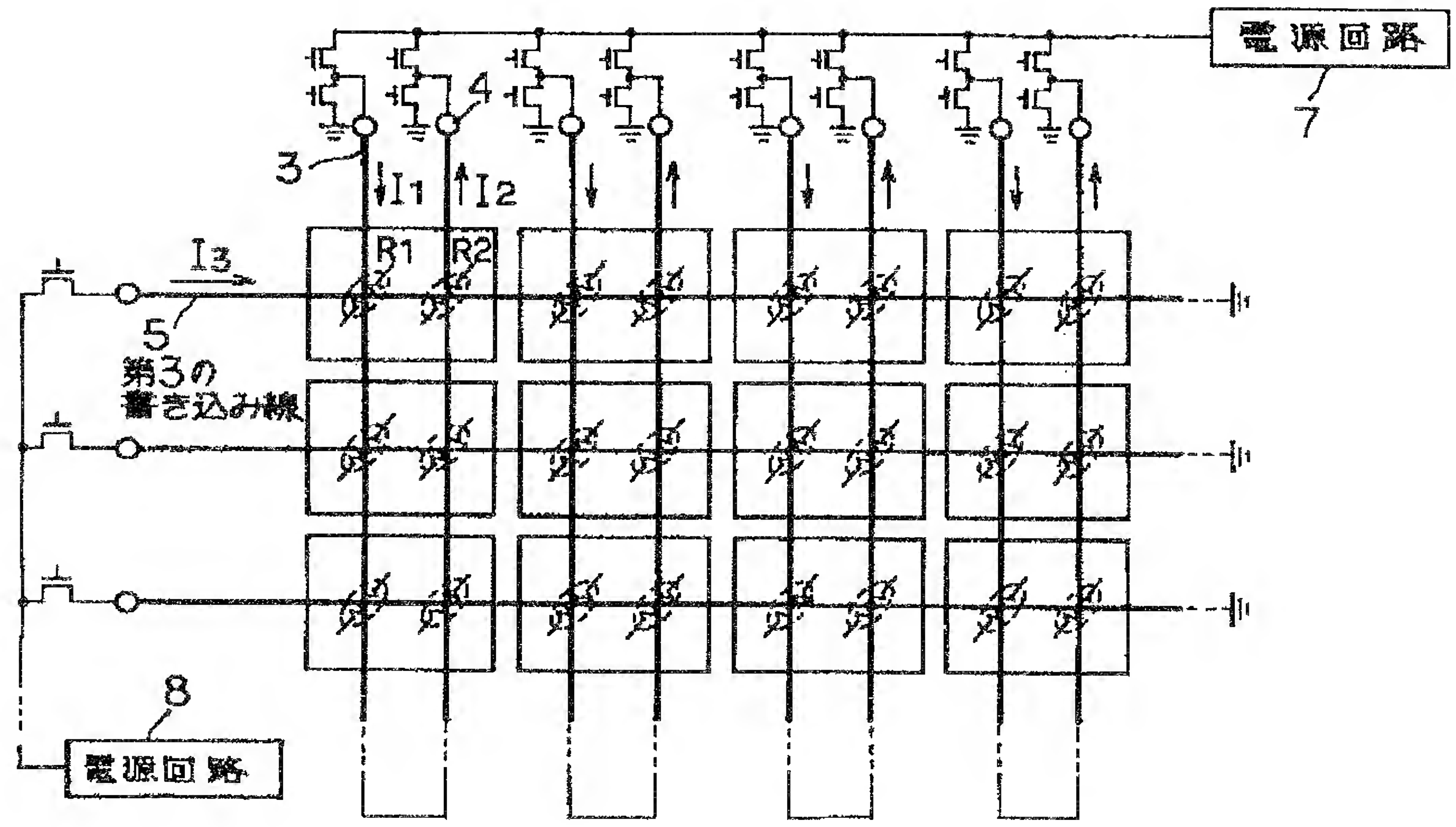
[Drawing 4]



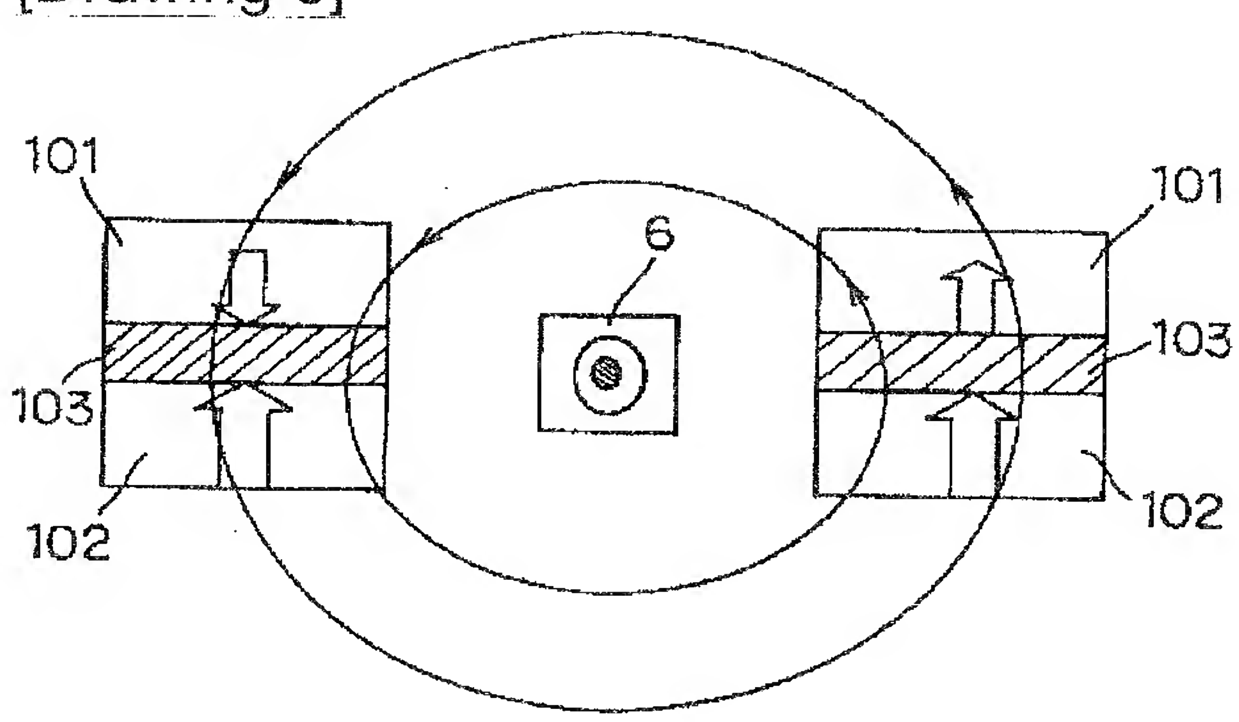
[Drawing 5]



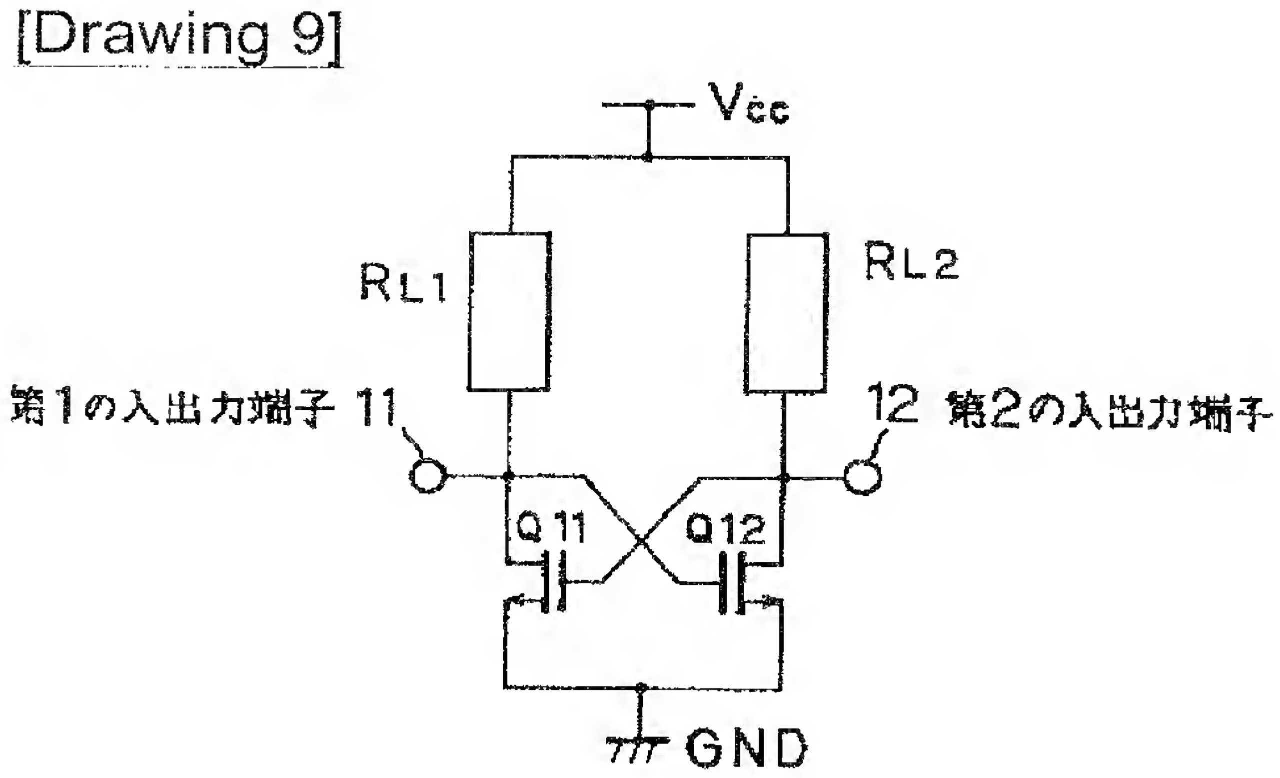
[Drawing 6]



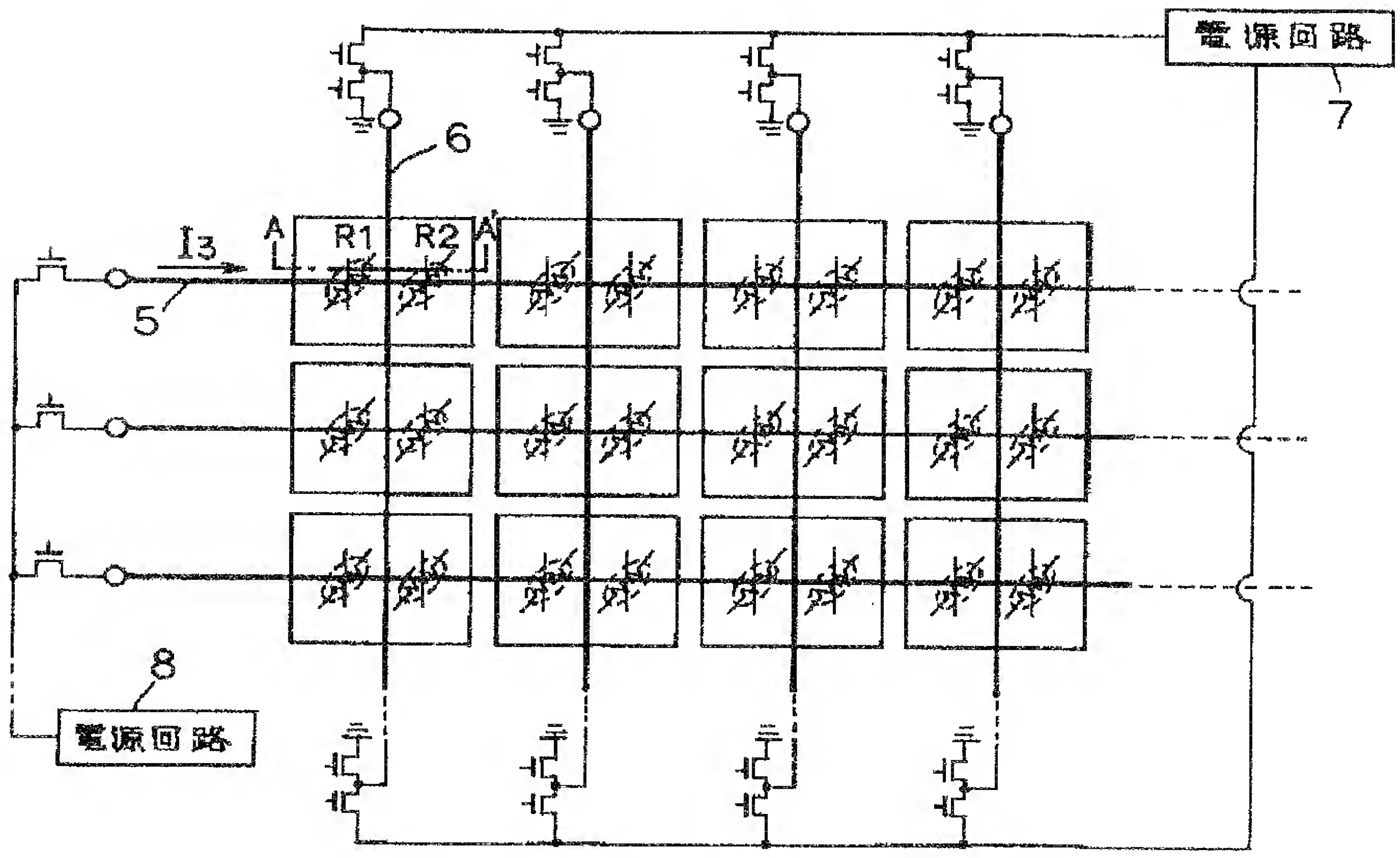
[Drawing 8]



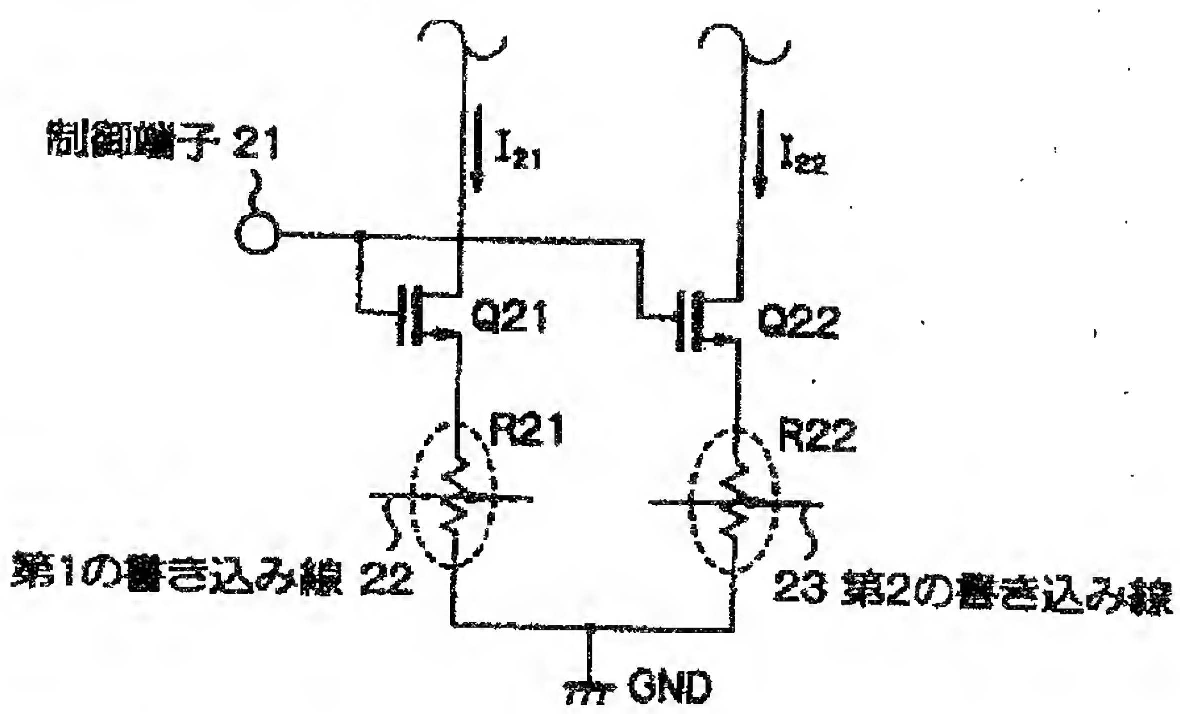
[Drawing 9]



[Drawing 7]



[Drawing 10]



[Translation done.]